#### **PCT**

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(71) Applicant: TEKSTAR SYSTEMS CORPORATION [US/US]; 2415 Parkview Road, Middleton, WI 53562 (US).

(72) Inventor: ELAM, Daryl, B.; 8503 Fairway Place, Middleton, WI 53562 (US).

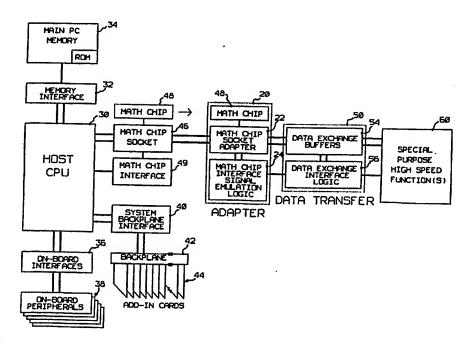
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(54) Title: INTERFACE SYSTEM FOR DATA TRANSFER WITH REMOTE PERIPHERAL INDEPENDENTLY OF HOST PROCESSOR BACKPLANE



(57) Abstract

Logic interface circuitry for bypassing the standard backplane bus (40) of a host computer (30) permits the transmission of data between the host computer (30) and special purpose high-speed function add-in peripherals (60). The data is transmitted at the rate it is generated by the host computer (30) and the add-in peripheral (60).

#### + DESIGNATIONS OF "SU"

It is not yet known for which States of the former Soviet Union any designation of the Soviet Union has effect.

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# INTERFACE SYSTEM FOR DATA TRANSFER WITH REMOTE PERIPHERAL INDEPENDENTLY OF HOST PROCESSOR BACKPLANE

#### BACKGROUND OF THE INVENTION

#### Field of the Invention

The invention relates to a means and method for bypassing standard computer interface backplanes in order to increase the data transfer rate between the host computer and a remote system.

#### Description of the Prior Art

It has long been recognized that the use of personal computers (PCs) is generally limited by their inability to perform certain functions in a high-speed, efficient manner. This leaves the users of certain special purpose high-speed function add-in peripherals with the choice of adapting to a slow, cumbersome processing operation, or of using a far more expensive mini-computer or mainframe system at many times the cost of a PC whenever efficiency and/or speed is a key factor in the operation.

The backplane bus bandwidth is the most significant factor in restricting the usefulness of high-speed add-in system components which require use of the backplane to communicate with a system central processing unit (CPU). Such components are most efficient when data transfer can be accomplished at the data transfer rate of the CPU rather than at the transfer rate of the backplane. The bandwidth limitations are most pronounced when there is a large discrepancy between the peak data transfer rate capabilities of the system CPU and the backplane bus. Over the years, this discrepancy has become greater and greater, as new generations of new CPUs are introduced far more often than new generations of backplane buses. As CPU capability and speed increase, the backplane becomes the limiting factor in using the CPU with add-in systems to perform more complex tasks.

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The primary reason that backplane design lags CPU development is the requirement for standardization. The Institute of Electrical and Electronic Engineers (IEEE) has established standards for backplane architecture which permit numerous manufacturers to design add-in systems for a variety of host CPUs with a high degree of certainty that the mixing and matching of such systems and CPUs will result in an operable system. While this approach assures flexibility, the tradeoff is a lack of efficiency.

In an effort to overcome this, more of the functions benefiting from high speed data transfer are being incorporated onto the host CPU board to avoid using the backplane bus as a communication device. Examples that have become accepted are numerics coprocessor chips, mass storage controllers, video controls and local network interfaces. Physical limitations of the host CPU board render continuing movement in this direction impractical, if not impossible.

The present invention is intended to permit a wide variety of add-in systems to operate at a high data transfer rate by bypassing the backplane of the host processor without the requirement that the add-in system be physically located on the CPU board. The invention takes advantage of the availability of the functional signals connected to and available at sockets generally provided in the standard CPU board. The invention uses the available sockets to permit development of a communications interface to shunt around the backplane bus. An adapter and data processing logic are connected to a selected data access point to provide a data transfer path for connecting the host CPU with the add-in systems. By

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add-in system.

using the invention, the data transfer rate can be increased by a factor approaching a magnitude over the capability of the backplane.

#### SUMMARY OF THE INVENTION

The present invention comprises a means and method for circumventing the limitations of the data communications speed of standard computer interface The backplane bus restricts the usefulness of a certain class of add-in system components, generally in the form of add-in circuit boards, which use the backplane bus to communicate with the system CPU. This class is characterized primarily by the desirability to tranfer data to and/or from the system CPU as quickly and efficiently as possible. The invention utilizes the standardization of the signal connections in the system CPU and/or other peripheral sockets in the CPU board as a convenient location to access the required signals and shunt around the system backplane bus. This may be accomplished by inserting a small socket adapter into the selected socket and then relocating the displaced chip into a similar socket provided on the adapter. In this manner, the protocol established between the displaced chip and the host CPU is maintained and the adapter borrows the data available from the CPU at the socket. Thus, the accessing schemes and handshake protocol of the original, now displaced chip are preserved and the host CPU operates as if it is communicating only with the chip.

In an alternative embodiment, the interface includes dedicated interface logic which duplicates the protocol and accessing schemes of the host CPU or the

socket by the adapter for communicating with the remote

signals which are available are then lifted from the

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displaced chip. This permits direct communication between the host CPU and the adapter circuitry without the use of the displaced chip.

The adapter provides a hard wired system which electrically connects the required signals available at the selected data access point to a remote add-in system to provide a high speed data transfer bus. The only additional electrical connections required other than those available at the selected socket may be the DC power and ground lines which can be taken directly from the standard backplane.

By way of example, the standard PC backplane, known as an Industry Standard Architecture (ISA) backplane, or alternatively, as the IBM PC-AT bus, provides a data path which is 16 parallel bits, the maximum recommended backplane clock speed being 8 megahertz (MHz). The fastest backplane transfers require 4 clock cycles, yielding a peak bandwidth of 4 megabytes per second. Using the present invention with a 33 MHz clock speed requires the same 4 clock cycles per transfer as is standard. The invention yields a data transfer rate of 33 megabytes per second, an over 8-fold improvement. In the example, an Intel 80386 The invention may be adapted microprocessor is used. to interface with most available microprocessors, numeric chips and other generally available sockets or access points, provided the CPU provides at the socket all signals required by the add-in board. The adapters may be stacked or "piggy-backed" on top of one another to permit multiple add-in boards simultaneously utilizing the same socket. The particular function of the add-in system is incidental to the invention as long as the signals required to operate the add-in system are available at the adapter socket.

The various advantages and features of the

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invention will be readily apparent from the accompanying drawings and description of the preferred embodiment.

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#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a general block diagram of a host processor in combination with a special purpose high-speed function peripheral add-in and an interface unit incorporating the teachings of the present invention.

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Fig. 2 is a detailed flow chart of the interface device illustrated in Fig. 1.

Fig. 3 is a diagram of a typical (prior art) state machine which may be an integral part of the interface device shown in Figs. 1 and 2.

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Figs. 4-13 are a schematic diagram of a data transfer interface device made in accordance with the teachings of the present invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENT

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As shown in Fig. 1, the present invention includes an adapter 20 and a data transfer device or circuit 50. In the embodiment illustrated, the CPU of a standard PC such as, by way of example, an IBM PC-AT compatible system having an Intel 80386 microprocessor 30, includes a standard memory interface 32 and main PC memory 34, typical onboard interfaces 36 and typical onboard peripherals 38. A standard system backplane interface 40 is used to provide communication between the CPU 30 and the backplane 42 for providing data transfer to and from the add-in cards 44.

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Typically, the PC will include numerous peripheral sockets such as, by way of example, the extended math chip (EMC) socket 46 adapted for receiving a standard numerics chip 48 such as, by way of example, the Weitek 3167 or the Intel 80387 math

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chip. The math chip interface logic circuitry 49 is also provided to control communication between the PC and the math chip.

The subject invention is specifically adapted for connecting the CPU 30 to special purpose high-speed function (SPHSF) add-in systems 60, bypassing the system backplane 42 by utilizing the direct connections to the full speed CPU signals via the math chip socket 46. The math chip socket of the CPU is a convenient place to gain access to the signals needed for the high-speed direct interface. However, the adapter could also be placed directly on the CPU chip or at any other convenient location on the main CPU circuit board where direct access to the required CPU signals can be gained.

As shown in Fig. 1, adapter 20 includes a math chip socket adapter 22 which is connected directly to the math chip socket via a standard plug and socket arrangement which is designed to mate with the math chip socket 46 provided in the PC. The adapter provides a direct communication link between the math chip socket and the data transfer device 50. The adapter can physically be plug compatible with the math chip socket and coupled to ribbon cables or the like which are, in turn, in direct communication with the data transfer device 50. As an option, the math chip 48 may be plug compatible with the adapter. The math chip interface logic 24 may be located on the adapter 20 or may be remote and coupled via the cable.

The protocol and accessing schemes provided in the math chip is preserved in one of three alternative methods when in utilizing the present invention. In the first, the math chip 48 is simply removed from the math chip socket and reinserted in the math chip socket adapter 22 in parallel with the data

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transfer logic device 50, whereby the PC continues to communicate directly with the math chip and the adapter "picks off" the signals in a passive or non-invasive manner and transmits them to the data transfer circuit 50. In the second method, the math chip interface signal emulation logic circuit 24 emulates the accessing and signal protocol scheme of the math chip to duplicate those of the math chip, whereby the CPU communicates with the adapter as if it were a math chip. In a third method and as described herein, the math chip is only emulated to the degree necessary to permit communication with the CPU. The system has distinct interface characteristics, only emulating as much as necessary of the math chip to permit communication.

The physical configuration of the socket adapter is not critical to the function of the invention except for the requirement that the pin and socket arrangement of the adapter must be compatible with the selected data access point on the CPU board. The adapter may be a structural part of the special purpose circuit board including the math chip interface signal emulation logic 24 and the data transfer logic 50, or it may be remote from the board and connected to it by using cables. Likewise, the SPHSF 60 may be plugged directly into the adapter and/or data transfer board or may be plugged into a socket which then communicates via cable with the data transfer board. The signals to be transmitted from the host CPU 30 to the SPHSF 60 are communicated to the data transfer device 50 via the adapter 20. The signals to be transmitted from the SPHSF 60 to the CPU 30 are communicated to the data transfer device 50 directly from the SPHSF 60. Data exchange buffers 54 receive the data at the rate it is generated and supply it to

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the receiving processor on demand at the rate it can be used. This permits use of asynchronous CPUs and SPHSF The data exchange interface logic device 56 provides interfacing and control logic for controlling the buffer function in response to the CPU 20 and SPHSF 60.

An expanded diagram of the data exchange circuitry 50 is illustrated in Fig. 2. As there shown, three primary communication paths exist between the adapter 20 and the data exchange circuitry 50. first is a host PC data bus 25 which directly links the CPU signals present at the math socket with the exchange circuitry 50. The host PC control bus 26 provides a path for communication of the various control signals between the CPU 30 and data exchange interface logic 56. In addition, PC address bus 27 and "selected" signal line 28 provide for the address and selection signals to be transmitted between the PC and the data exchange circuitry via adapter 20. The data transfer and control signals between the data exchange circuit 50 and the SPHSF 60 are provided at buses 51 and 52 and 33, respectively. The data transfer rate is at the respective processing rate of the SPHSF 60 and the host CPU 30. By using this scheme, the CPU and the SPHSF can transfer data to and from each other at the speed of each of the systems, rather than at the speed permitted by standard backplane architectures.

By way of example, by using the adapter 20 and the data transfer circuitry 50 of the present invention, an over 800% advantage can be gained in data transfer rate (DTR) over that available from a standard IBM PC-AT bus. Using the following formula to determine data transfer rate in megabytes per second (MBs):

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DTR =  $\frac{RxWx(1-L)}{Cx8}$ , where

R = the bus clock rate in megahertz,

W = the width of the data bus in bits,

L = the loss due to refresh,

C = clock periods per transfer, and

8 = the number of bits per byte.

instructions are used for data transfer and that these are the "string move" instructions of the Intel 386 CPU for an IBM PC-AT such as, by way of example, "REP MOVSW", and the effects of the PC main memory refresh are equal in both cases, the following calculations can be made:

#### For the PC-AT Bus:

 $DTR = \frac{RxWx(1-L)}{Cx8}$ 

 $= \frac{8 \times 16 \times (1 - .03)}{4 \times 8}$ 

= 3.88 mbs

#### Data Exchange of the Invention:

 $DTR = \frac{RxWx(1-L)}{Cx8}$ 

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33x32x(1-.03) 4x8

= 32.01 mbs

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Thus, for the specific example, the invention provides an increase in data transfer rate of

32.01 3.88 , or 825%

Basically, the data exchange circuit 50 operates as a buffer for storing data produced by the host CPU 30 and the SPHSF 60. The buffers 54 collect information as quickly as it is produced and release it on demand, as needed. The interface logic 56 monitors the SPHSF 60 and the buffers 54 to determine when the buffers are ready to receive data and when the buffers have data available to transfer relative to the SPHSF. The host CPU interface logic 57 communicates with the math chip socket adapter and through it with the host CPU 30 to similary monitor and determine when the buffers are ready to receive and/or transfer data relative to the host CPU.

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With specific reference to the exchange buffers 54, the preferred embodiment employs two FIFO registers 100, 102. The FIFO 100 receives data from the host CPU 30 via the adapter 20 and makes it available to the SPHSF 60. The FIFO 102 receives data from the SPHSF 60 and makes it available to the host

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CPU 30 via the adapter 20. The dual port RAM 104 which allows both the host CPU 30 via the socket adapter 20 and/or the SPHSF 60 to read and write data autonomously and asynchroncusly in at random addresses. The dual port RAM provides substantial flexibility in the data exchange sequence. The SPHSF, for example, accesses stored data at random as needed, or can "look" at data in the RAM without deleting it. The host can, for example, enter and change commands in the RAM whether or not the SPHSF ever accesses or utilizes the them. The FIFOs are each one-way circuits, as their name implies, and whatever data goes in, comes out in the same order.

If the SPHSF is of the type including a programmable component such as a microprocessor, then the host CPU is adaptable to provide instruction codes to the programmable component via the data exchange circuitry. Specifically, the data exchange circuitry is operable to transfer not only operand data but instruction codes and commands, as well.

In order to make the transfer scheme functional when plugged into the math chip socket, the data exchange circuitry must be able to communicate with the host CPU 30. This can be accomplished by using one of the three following methods:

The numerics chip may be plugged into the adapter, whereby the CPU 30 continues to communicate directly with the numerics chip and the data available at the adapter is lifted from the chip socket for use by the data exchange circuitry and the SPHSF;

(2) The math chip interface signal emulation logic circuitry 24 includes logic for duplicating

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the protocol and accessing schemes of the numerics chip to simulate the identity of the numerics chip, permitting the host CPU 30 to function as if it were communicating directly with a standard numerics chip; or

distinct identity provided that specific signals present in the math chip are handled in a manner compatible with the host CPU, i.e., the interface emulates the selected, required minimum protocol of the math chip while ignoring superfluous signals not relevant to the SPHSF.

An example for providing signal emulation is incorporated in the state machine shown in Fig. 3 which is the architecture for a typical state machine for the Intel 80386 microprocessor is illustrated in Fig. 3. The information for creating the state machine is directly available from the Intel 80386 Users Manual. The state machine logic is loaded into PLD circuits provided in the math chip CPU control logic circuitry 108. The math chip CPU control logic circuit communicates directly with the host CPU 30 through the math chip socket adapter 20 and emulates protocol and accessing schemes of a numerics chip, permitting the CPU 30 to function as if it were communicating with the numerics chip.

The math chip CPU control logic 108 communicates directly with the math chip socket to provide emulation. The address decoder is standard decoder architecture similar to that used in the numerics chip or other add-in function peripherals and provides the required handshaking signals between the peripheral and the host CPU 30.

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The SPHSF 60 can be any special purpose highspeed functional peripheral. The SPHSF may include a CPU 120 which is adapted for receiving and sending data signals to and from the host CPU 30. In the prior art systems, the SPHSF would have to communicate directly with the host processor through the standard backplane. Where the SPHSF was capable of providing high-speed functions, the system efficiency was entirely dependent upon the speed of the backplane. By using the subject invention, the data exchange circuitry can receive data between the SPHSF 60 and the host CPU 30 at the speed it is generated and supply on demand, as needed. The peak data transfer rate is the data utilization rate of the SPHSF. The SPHSF interface logic circuit 56 in the data exchange circuitry would be customized for each specific The SPHSF may be expandable and adapted to include additional peripherals, as illustrated by DRAM

It will be readily appreciated that the use of the data transfer scheme of the present invention permits utilization of special purpose high-speed functional add-in peripherals with stand alone computer systems, wherein the rate of data transfer between the SPHSF and the host computer is limited only by the speed at which both the host processor and the add-in peripheral generate and utilize data, rather than being limited by standard backplane architecture. This permits the user to buy a relatively inexpensive PC or other microprocessor based host system and add to it the data transfer system of the present invention for substantially less investment than required to purchase a mini-computer or a mainframe, permitting performance levels at mini-computer or mainframe speeds. For

example, using the invention with a PC having an Intel

control 122 and DRAM expansion board 124.

386 microprocessor and an SPHSF includes an Intel 80860 microprocessor, numerical processing sequences can be performed at about half the rate of a CRAY-1 supercomputer at less than 1% of the cost.

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A detailed schematic diagram of a data transfer interface device made in accordance with the present invention is illustrated in Figs. 4-13. illustrated, the cable connectors provide direct access to the host CPU signals and to other useful signals which can be utilized to provide the optimum interface between the host and the add-in SPHSF. In Fig. 4, the upper PLD Ul implements a state machine which tracks the state machine of the host CPU (Fig. 3) by monitoring the signals available via the cable from the adapter. The upper PLD also implements the required handshaking signals according to the host CPU's required protocol for the transfer of data to and from the host. The lower PLD U2 implements the control signals used to interface with the data exchange buffers and other control logic.

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In Fig. 5, the PLD U3 implements the control logic for the exchange of data from the host CPU's side of the data exchange buffers. In this case, they control reading from and writing to FIFO and random access dual port memories. The other side of the FIFOs and dual port memories is written to or read from by the SPHSF. The PAL U4 performs the same functions as the PAL U3 except that this PAL performs it's functions on behalf of the SPHSF, and thus is connected to the logically opposite side of the various buffers and control circuits.

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In Fig. 6, the four cable connectors P4, P5, P6 and P7 carry the host CPU data bus signals to and from the host CPU socket adapter. In this design there are 32 host data bits, but if there were more or fewer

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data bits, then the number of buffer logic chips would simply be adjusted to the required number to match the data bus width of the host CPU. The signals on the right side of Fig. 6 are the latched data bus bits from the host CPU or the unlatched data bus bits from the data exchange buffers.

The FIFO circuits in Fig. 7 comprise the lower 32 bits of the SPHSF data bus, which are also the even 32 bit words of the host CPU. These FIFOs pass data unidirectionally from the host to the SPHSF. FIFO circuits in Fig. 8 comprise the upper 32 bits of the SPHSF data bus, which are also the odd 32 bit words of the host CPU. These FIFOs pass data unidirectionally from the host to the SPHSF. circuits in Fig. 9 comprise the lower 32 bits of the SPHSF data bus, which are also the even 32 bit words of the host CPU. These FIFOs pass data unidirectionally from the SPHSF to the host. The FIFO circuits in Fig. 10 comprise the upper 32 bits of the SPHSF data bus, which are also the odd 32 bit words of the host CPU. These FIFOs pass data unidirectionally from the SPHSF to the host.

The dual port RAM chips U25 and U26 in Fig. 11, and U27 and U28 in Fig. 12 are each one megabit memories organized as 64K by 16 bits and are of the fully asynchronous dual ported variety. All signals on the left sides of the chips are connected to the host CPU and/or host interface control circuitry, and vise versa, all signals on the right side are connected to the SPHSF. This provides a random access memory for applications and algorithms not well suited for the sequential nature of FIFOs. The RAMS U25 and U26 from the lower 32 bits and the RAMS U27 and U28 from the upper 32 bits of the dual port RAM 104.

The dual port RAM chips U27 and U28 in Fig.

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12 are each one megabit memories organized as 64K by 16 bits and are of the fully asynchronous dual ported variety. All signals on the left sides of the chips are connected to the host CPU and/or host interface control circuitry, and vice versa, all signals on the right side are connected to the SPHSF unit. This provides a random access memory for applications and algorithms not well suited for the sequential nature of FIFOs.

The SPHSF shown in Fig. 13 is shown merely as an example and is a 64 bit high speed RISC processor which is to be used primarily as an accelerator for numerical computation intensive applications. The high speed interface to the host could be utilized for virtually any special function which would benefit from high data transfer rates. Examples would be mass storage controllers, signal processing sub-systems, image processors and the like.

While certain features and embodiments of the invention have been described herein, it will be understood that the invention includes all alternatives encompassed within the scope and spirit of the following claims.

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#### CLAIMS

#### What is claimed is:

- l. A host/peripheral interface for providing the transfer of data between a host processor and a remote special purpose high-speed system, the transfer means comprising:
- a. an adapter for connecting said interface directly to a data access point associated directly with the host processor;
- b. logic means in communication with the adapter for establishing protocol and access schemes acceptable to the host processor for signaling the host processor to send and receive data at the data access point; and
- c. a data transfer device in direct communication with the adapter and the remote system for transmitting data between the host processor and the remote system at a data transfer rate equal to the rate said data is generated by the respective host processor and/or remote system.
- 2. The host/peripheral interface of Claim 1, the data transfer device further comprising:
- a. a first buffer means in communication with the adapter and the remote system for receiving data generated by the host processor and for storing the data for release to or use by the remote system on an as-needed basis: and
- b. a second buffer means in communication with the remote system and the adapter for receiving data generated by the remote system and for storing the data for release to or use by the host processor; and
- 3. The host/peripheral interface of Claim 2, further including a data exchange logic device in communication with the adapter, the remote system and the buffer means for signaling to each buffer means

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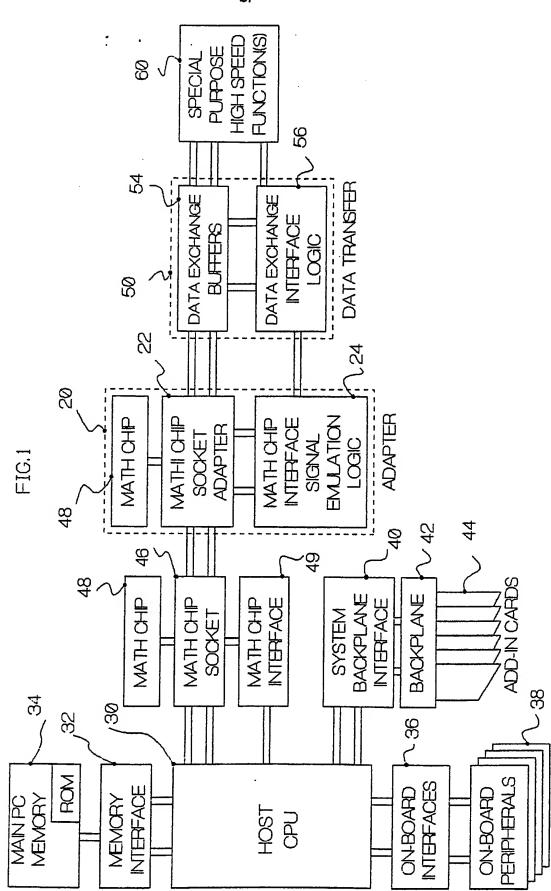
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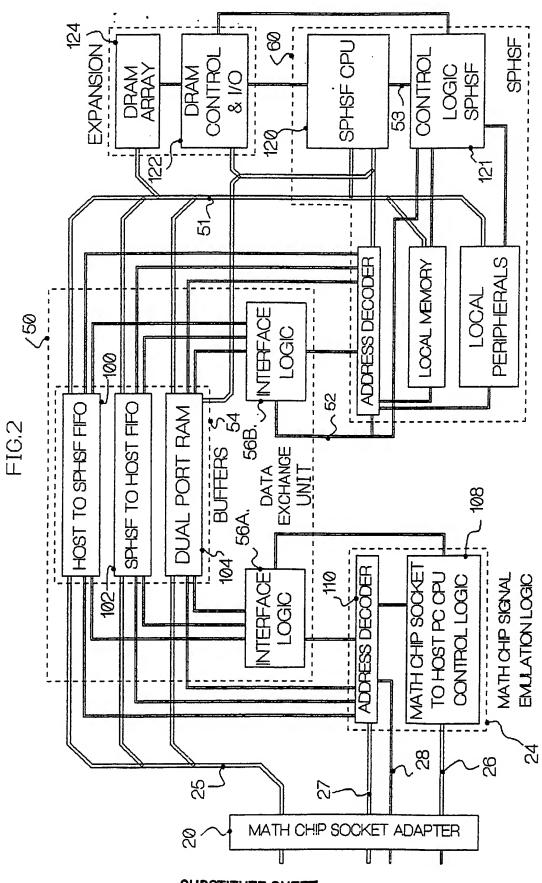
- when the remote system is ready to use or receive the data stored in the respective buffer means.
  - 4. The host/peripheral interface of Claim 2, wherein each buffer means further comprises:
  - a. a first-in, first-out data storage
    .device; and
  - b. a dual port memory in communication with the adapter and the host processor and the remote system.
  - 5. The host/peripheral interface of Claim 4, each first-in, first-out register having a 512x64 configuration.
  - 6. The host/peripheral interface of Claim 3, the host of the type generating control signals separate and distinct from the data signals, the data exchange logic device further comprising a control logic means for receiving the control signals and transmitting said control signals to the respective buffer means.
  - 7. The host/peripheral interface of Claim 1, the host processor of the type including a standard extended math chip socket, the adapter further including means for connecting said interface device directly into said extended math chip socket.
  - 8. The host/peripheral interface of Claim 7, the extended math chip socket connecting means further including means for connecting a numerics chip in the extended math chip socket in parallel with said host/peripheral interface device.
  - 9. The host/peripheral interface of Claim 7, the logic means further including means for emulating the protocol and accessing schemes of a standard numerics chip.
  - 10. A method for bypassing the backplane of a host processor when transmitting data between the host

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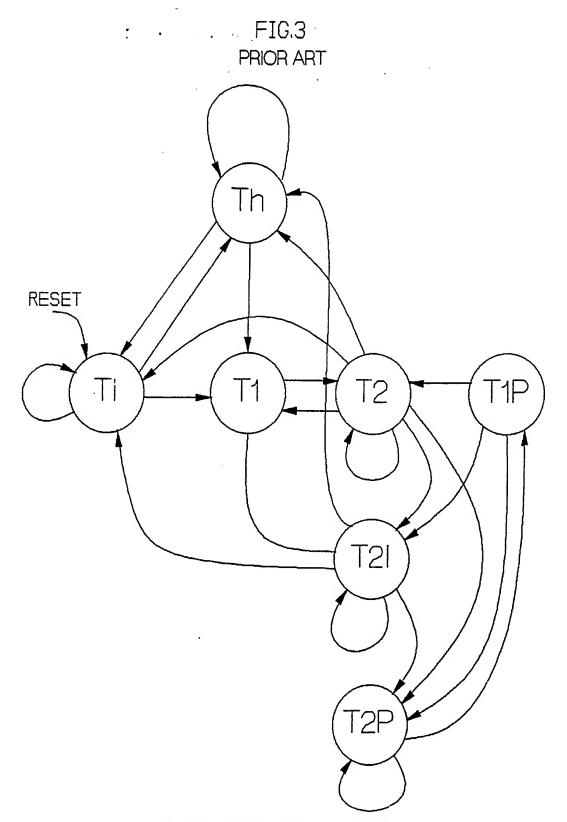
processor and a remote special purpose high-speed addin system, comprising the steps of:

- a. selecting a data access point on the host processor;
  - b. emulating the protocol and access schemes required for the host processor to send and receive data to the access point;
- 10 c. collecting and storing data generated and transmitted by the host processor and the remote system; and
  - d. using the stored data.
  - 11. The method according to Claim 10, the host processor of the type including an extended math chip socket, wherein the signals generated and transmitted by the host processor are collected at said socket, and wherein the signals generated and transmitted by the remote system are transmitted to said socket.



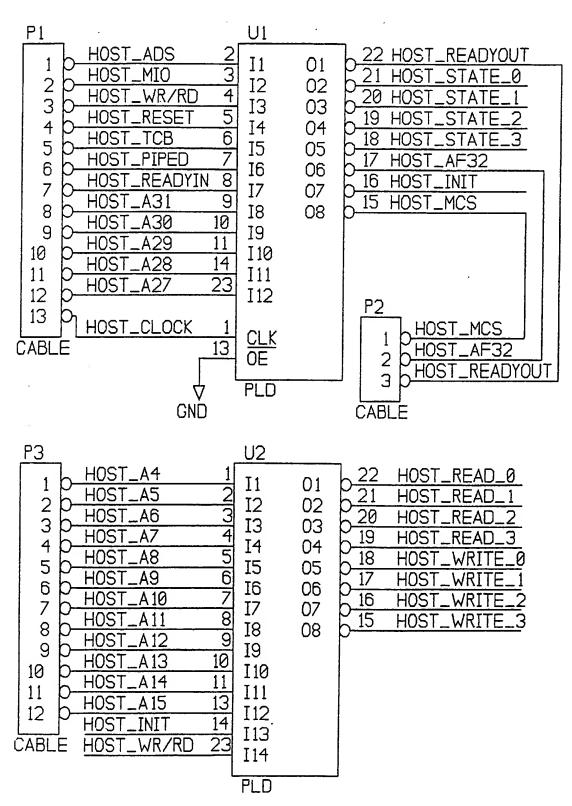


SUBSTITUTE SHEET



386 DX COMPLETE BUS STATES (INCLUDING PIPELINED ADDRESS)

FIG.4



HOST I/O CONTROL LOGIC

SUBSTITUTE SHEET

DATA EXCHANGE LOGIC

PLD

I11

**I12** 

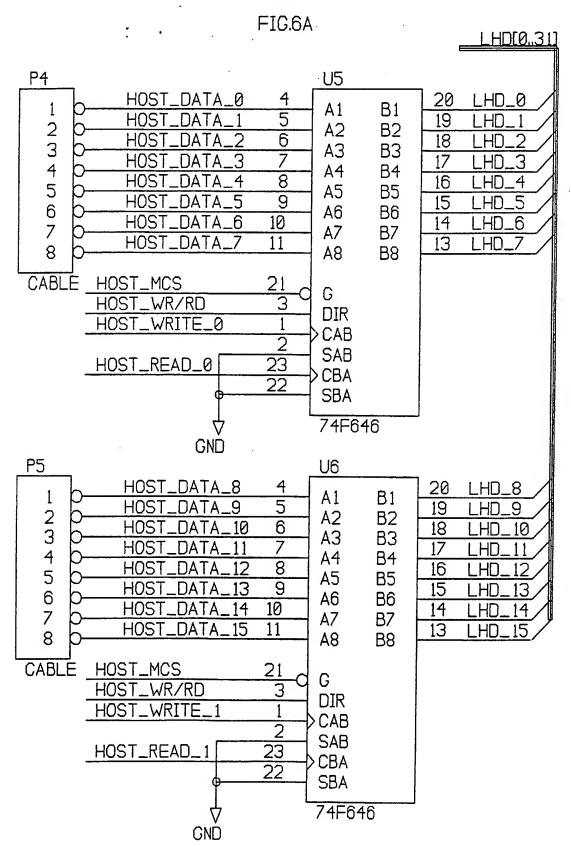
I13

I14

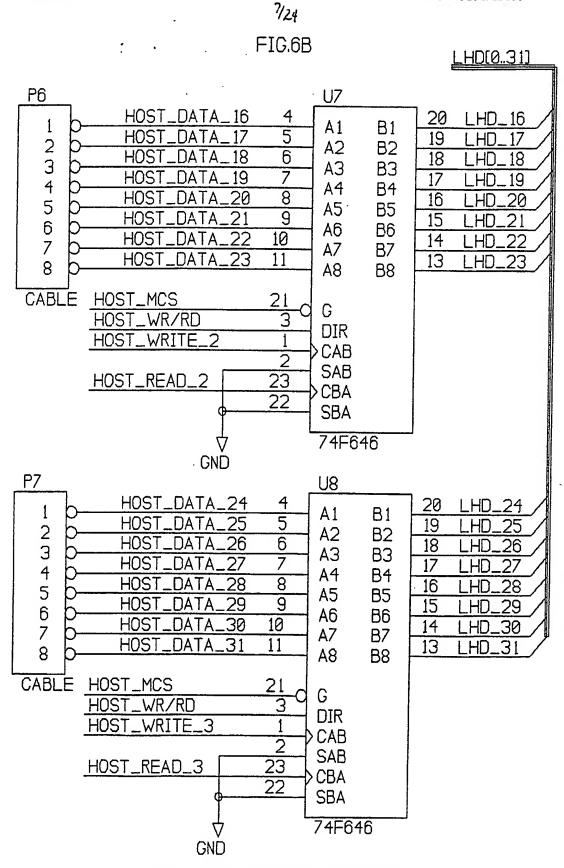
13 SPHSF\_A29

14 SPHSF\_A30

23 SPHSF\_A31



HOST DATA EXCHANGE REGISTERS



HOST DATA EXCHANGE REGISTERS

: · FIG.7A

	`L10'\	$\sqcap$
HOST_DATA_[031]		SPHSF_DATA_[063]
	<u>U9</u>	·
LHD_1 LHD_2 LHD_3 LHD_4 2 LHD_5 2 LHD_6 2 LHD_7 2	6 05	9 SPHSF_DATA_0 / 10 SPHSF_DATA_1 / 11 SPHSF_DATA_2 / 12 SPHSF_DATA_3 / 16 SPHSF_DATA_4 / 17 SPHSF_DATA_5 / 18 SPHSF_DATA_6 / 19 SPHSF_DATA_7 / 08 / 13
HOST_RESET 2 SPHSF_FIFO_READ_01 HOST_FIFO_WRITE_0	7 XI 23 FL/RT RST RCLK WCLK 7201	XO/HF 20 21 SPHSF_FIFO_EMPTY FF 8 SPHSF_FIFO_FULL
LHD_9 :		Q0
HOST_RESET 2 SPHSF_FIFO_READ_01 1 HOST_FIFO_WRITE_0	7 XI	XO/HF 20 EF 21 FF 8

HOST TO SPHSF FIFO BITS 0 TO 15

HOST\_RESET

SPHSF\_FIFO\_READ\_01

HOST\_FIFO\_WRITE\_0

WO 92/01987 PCT/US91/05006 9/24 FIG.7B SPHSF\_DATA\_[0,63] HOST\_DATA\_[0,.31] U11 9 SPHSF\_DATA\_16 LHD\_16 DØ Q0 SPHSF\_DATA LHD\_17 D1 Q1 SPHSF\_DATA LHD\_18 Q2 D2 12 SPHSF\_DATA LHD\_19 Q3 D3 LHD\_20 16 SPHSF\_DATA D4 Q4 26 LHD\_21 17 SPHSF\_DATA **D**5 Q5 25 LHD\_22 SPHSF\_DATA 18 D6 Q6 24 LHD<sub>23</sub> 19 SPHSF\_DATA. D7 Q7 2 13 **D8** Q8 XO/HF FL/RT EF HOST\_RESET RST FF SPHSF\_FIFO\_READ\_0115 >RCLK HOST\_FIFO\_WRITE\_0 > WCLK 7201 U12 9 SPHSF\_DATA LHD\_24 DØ Q0 LHD\_25 SPHSF\_DATA DI Q1 LHD\_26 SPHSF\_DATA Q2 D2 \_27 SPHSF\_DATA LHD\_ D3 Q3 SPHSF\_ \_28 16 .DATA **D4** Q4 LHD\_29 26 17 SPHSF\_DATA D5 Q5 25 LHD\_30 18 SPHSF\_ .DATA 30 D6 Q6 24 19 SPHSF\_ DATA LHD\_31 D7 Q7 13 **D8** Q8 20 XI XO/HF

HOST TO SPHSE FIFO BITS 16 TO 31

FL/RT

RST

>RCLK

>WCLK

7201

21

8

EF

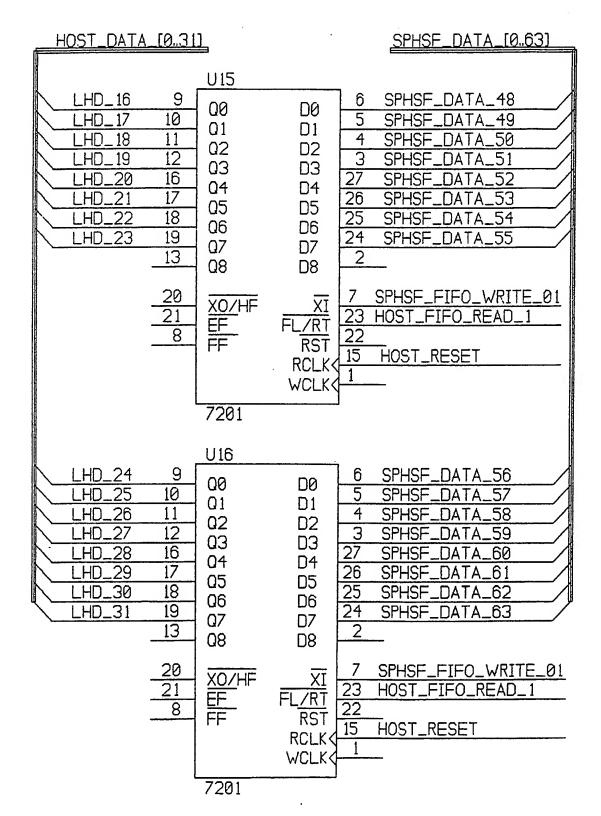
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: · FIG.8A

HOST_DATA_[031]			SPHSF_DATA_[063]
LHD_0 9 LHD_1 10 LHD_2 11 LHD_3 12 LHD_4 16 LHD_5 17 LHD_6 18 LHD_7 19	00 01 02 03 04 05 06 07 08	D0 6 D1 4 D2 3 D3 27 D4 26 D5 25 D6 24 D7 2	SPHSF_DATA_32 SPHSF_DATA_33 SPHSF_DATA_34 SPHSF_DATA_35 SPHSF_DATA_36 SPHSF_DATA_37 SPHSF_DATA_38 SPHSF_DATA_38
HOST_FIFO_EMPTY_1 21 HOST_FIFO_FULL_1 8	XO/HF EF FF 7201	PCI V 15	HOST_RESET HOST_FIFO_READ_1 SPHSF_FIFO_WRITE_01
LHD_8 9 LHD_9 10 LHD_10 11 LHD_11 12 LHD_12 16 LHD_13 17 LHD_14 18 LHD_15 19	01 02 03 04 05 06 07 08	D0 6 5 4 D2 3 27 D4 26 D5 D6 D7 D8 D8	SPHSF_DATA_40 · SPHSF_DATA_41 SPHSF_DATA_42 SPHSF_DATA_43 SPHSF_DATA_44 SPHSF_DATA_45 SPHSF_DATA_45 SPHSF_DATA_46 SPHSF_DATA_47
20 21 8	XO/HF EF FF 7201	RCI K 15 I	- HOST_RESET HOST_FIFO_READ_1 PHSF_FIFO_WRITE_01

SPHSF TO HOST FIFO BITS 32 TO 47

FIG.8B



SPHSF TO HOST FIFO BITS 48 TO 63

i<sup>2</sup>/<sub>24</sub> : FIG.9A

HOST_DATA_[0,31]		SPHSE_DATA_[0,63]
LHD_0 9 LHD_1 10 LHD_2 11 LHD_3 12 LHD_4 16 LHD_5 17 LHD_6 18 LHD_7 19 13	017 00 01 02 03 04 05 06 07 08	D0 6 SPHSF_DATA_0 D1 5 SPHSF_DATA_1 D2 3 SPHSF_DATA_2 D3 27 SPHSF_DATA_3 D4 26 SPHSF_DATA_5 D5 25 SPHSF_DATA_6 D7 2 SPHSF_DATA_7 D8 2
HOST_FIFO_EMPTY 21 HOST_FIFO_FULL 8	XO/HF EF FF 7201	TI 7 23 FL/RT 22 HOST_RESET RST 15 HOST_FIFO_READ_0 WCLK 1 SPHSF_FIFO_WRITE_01
LHD_8 9 LHD_9 10 LHD_10 11 LHD_11 12 LHD_12 16 LHD_13 17 LHD_14 18 LHD_15 19	U18 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	D0 6 SPHSF_DATA_8 D1 4 SPHSF_DATA_9 D2 3 SPHSF_DATA_10 D3 27 SPHSF_DATA_11 D4 26 SPHSF_DATA_13 D5 25 SPHSF_DATA_14 D7 24 SPHSF_DATA_15 D8
20 21 8	X0/HF EF FF 7201	FL/RT 23  FL/RT 22 HOST_RESET  RCLK 1 SPHSF_FIF0_WRITE_01

SPHSF TO HOST FIFO LOWER BITS 0 TO 15

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: FIG.9B

HOST_DATA_[0.	311		SPHSE_DATA_[0,,63]
LHD_16 9 LHD_17 10 LHD_18 11 LHD_19 12 LHD_20 16 LHD_21 17 LHD_22 18 LHD_23 19 13	U19 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	DØ D1 D2 D3 D4 D5 D6 D7	6 SPHSF_DATA_16 5 SPHSF_DATA_17 4 SPHSF_DATA_18 3 SPHSF_DATA_19 27 SPHSF_DATA_20 26 SPHSF_DATA_21 25 SPHSF_DATA_22 24 SPHSF_DATA_23 2
20 21 8	7201 U20	XI FL/RT RST RCLK < WCLK <	7 23 22 HOST_RESET 15 HOST_FIFO_READ_0 1 SPHSF_FIFO_WRITE_01
LHD_24 9 LHD_25 10 LHD_26 11 LHD_27 12 LHD_28 16 LHD_29 17 LHD_30 18 LHD_31 19 13	QØ Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	D0 D1 D2 D3 D4 D5 D6 D7 D8	6 SPHSF_DATA_24 5 SPHSF_DATA_25 4 SPHSF_DATA_26 3 SPHSF_DATA_27 27 SPHSF_DATA_28 26 SPHSF_DATA_29 25 SPHSF_DATA_30 24 SPHSF_DATA_31 2
20 21 8	X0/HF EF FF 7201	XI FL/RT RST RCLK WCLK	7 23 22 HOST_RESET 15 HOST_FIFO_READ_0 1 SPHSF_FIFO_WRITE_01

SPHSF TO HOST FIFO LOWER BITS 16 TO 31

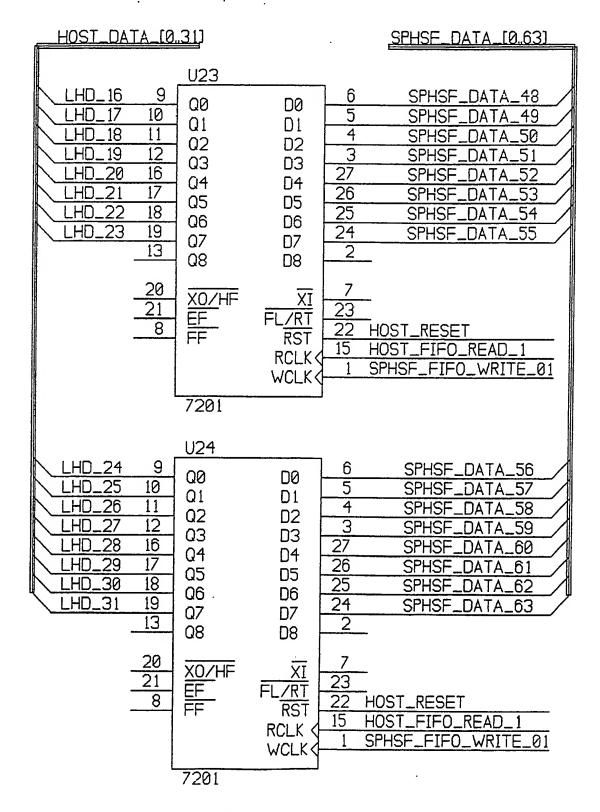
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: FIG.10A

HOST_DATA_[0,:31]_		SPHSF_DATA_[0,63]
LHD_0 9 LHD_1 10 LHD_2 11 LHD_3 12 LHD_4 16 LHD_5 17 LHD_6 18 LHD_7 19	U21 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	D0 6 SPHSF_DATA_32 5 SPHSF_DATA_33 4 SPHSF_DATA_34 D2 3 SPHSF_DATA_35 D3 27 SPHSF_DATA_36 D5 26 SPHSF_DATA_37 D6 25 SPHSF_DATA_38 D7 27 SPHSF_DATA_38 D7 28 SPHSF_DATA_39 D8 2
HOST_FIFO_EMPTY_1 21 HOST_FIFO_FULL_1 8	XO/HF EF FF 7201	TI 7 23 FL/RT 22 HOST_RESET RST 15 HOST_FIFO_READ_1 WCLK 1 SPHSF_FIFO_WRITE_01
LHD_8 9 LHD_9 10 LHD_10 11 LHD_11 12 LHD_12 16 LHD_13 17 LHD_14 18 LHD_15 19	U22 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	D0 6 SPHSF_DATA_40 D1 5 SPHSF_DATA_41 D2 4 SPHSF_DATA_42 D3 3 SPHSF_DATA_43 D4 26 SPHSF_DATA_44 D5 26 SPHSF_DATA_45 D6 27 SPHSF_DATA_46 D7 28 SPHSF_DATA_47 D8 2
20 21 8	X0/HF EF FF 7201	TI 7 FL/RT 23 FL/RT 22 HOST_RESET RCLK 15 HOST_FIFO_READ_1 WCLK 1 SPHSF_FIFO_WRITE_01

SPHSF TO HOST FIFO BITS 32 TO 47

FIG.10B



SPHSF TO HOST FIFO BITS 48 TO 63

: . FIG.11A

HOST_DATA_[0,.31]				CRUCE DATA (0.63)
				SPHSF_DATA_[0.63]
H0ST_A[0,.31]				SPHSF_A[0,31]
	<u>U25</u>	<del></del>		
HOST_A0	AA0		BA0	SPHSF_A0
HOST_A1	AA1		BA1	SPHSF_A1
HOST_A2	AA2		BA2	SPHSF_A2
HOST_A3			BA3	SPHSF_A3
HOST_A4 HOST_A5	HAA4 AA5		BA4 BA5	SPHSF_A4 SPHSF_A5
HOST_A6	AA6		BA6	SPHSF_A6
HOST_A7	AA7		BA7	SPHSF_A7
HOST_A8	BAAL_		BA8	SPHSF_A8
HOST_A9	AA9	6	BA9 BA10	SPHSF_A9
HOST_A11		_	BA11	SPHSF_A10
HOST_A12		4	BA 12	SPHSF_A12
HOST_A13	_	K	BA13	SPHSF_A13
HOST_A14		• •	BA 14	SPHSF_A14
HOST_A15	AA 15		BA 15	SPHSF_A15
		X		
HOST_RAM_READ_0	ARD		BRD	SPHSF_RAM_READ_01
HOST_RAM_WRITE_0	AWR	1	BWR	SPHAF_RAM_WRITE_01
LUDA	ADO.	7	DDG	CRUCE DITI
LHD_0 LHD_1	AD0 AD1	6	BD0 BD1	SPHSF_DATA_0 SPHSF_DATA_1
LHD_2	AD2		BD2	SPHSF_DATA_2
LHD_3	AD3		BD3	SPHSF_DATA_3
LHD_4	AD4		BD4	SPHSF_DATA_4
LHD_5 LHD_6	AD5		BD5	SPHSF_DATA_5
LHD_7	AD6 AD7		BD6 BD7	SPHSF_DATA_6 SPHSF_DATA_7
LHD_8	AD8		BD8	SPHSF_DATA_8
LHD_9	AD9		BD9	SPHSF_DATA_9
LHD_10	AD10		BD10	SPHSF_DATA_10
LHD_11 LHD_12	AD11 AD12		BD11 BD12	SPHSF_DATA_11
LHD_12	AD12		BD 13	SPHSF_DATA_12 SPHSF_DATA_13
LHD_14	AD14		BD14	SPHSF_DATA_14
LHD_15	AD15		BD 15	SPHSF_DATA_15
74.5				
#H				
	DUAL_	PORT	RAM	

DUAL PORT RAM BITS 0 TO 15

'7/<sub>24</sub>: FIG.11B

			7,110		
HOST	DATA_[031]_			SPHSF_DATA_[0.63]	
HOST	A[031]		•	SPHSF_A[0,31]	
	U2	26			
	HOST_A0 AA HOST_A1 AA HOST_A2 AA HOST_A3 AA HOST_A5 AA HOST_A6 AA HOST_A7 AA HOST_A8 AA HOST_A9 AA HOST_A10 AA HOST_A11 AA HOST_A12 AA HOST_A13 AA	12 13 14 15 16 17 18 19 11 11 12	BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7 BA8 BA10 BA11 BA12 BA13	SPHSF_A0 SPHSF_A1 SPHSF_A2 SPHSF_A3 SPHSF_A4 SPHSF_A5 SPHSF_A6 SPHSF_A7 SPHSF_A8 SPHSF_A9 SPHSF_A9 SPHSF_A10 SPHSF_A11 SPHSF_A12 SPHSF_A13	
	HOST_A14 AA	1	BA14	SPHSF_A13	
	HOST_A15 AA	15	BA 15	SPHSF_A15	
	·	X			
	_RAM_READ_0 ARE _RAM_WRITE_0 AW		BRD BWR	SPHSF_RAM_READ_01 SPHAF_RAM_WRITE_01	
	LHD_16 ADC LHD_17 ADC LHD_18 ADC LHD_19 ADC LHD_21 ADC LHD_21 ADC LHD_23 ADC LHD_24 ADC LHD_25 ADC LHD_26 ADC LHD_27 ADC LHD_27 ADC LHD_28 ADC LHD_29 ADC LHD_30 ADC LHD_30 ADC LHD_31 ADC LHD_31 ADC LHD_31	1 2 3 4 5 5 7 8 9 0 1 2 3 4	BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7 BD8 BD10 BD11 BD12 BD13 BD14 BD15	SPHSF_DATA_16 SPHSF_DATA_17 SPHSF_DATA_18 SPHSF_DATA_19 SPHSF_DATA_20 SPHSF_DATA_21 SPHSF_DATA_21 SPHSF_DATA_22 SPHSF_DATA_22 SPHSF_DATA_23 SPHSF_DATA_24 SPHSF_DATA_25 SPHSF_DATA_26 SPHSF_DATA_26 SPHSF_DATA_27 SPHSF_DATA_28 SPHSF_DATA_29 SPHSF_DATA_30 SPHSF_DATA_31	
	DUA	L_PORT_	RAM		

DUAL PORT RAM BITS 16 TO 31

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,,,,	

	F	IG.1	L2A	
HOST_DATA_[0,,31]	•			SPHSF_DATA_[0,,63]
H0ST_A[0,:31]				SPHSF_A[0,31]
HUS1_ALUS11	<u>U27</u>			I SI HSE_ALOSII
HOST_A0 HOST_A1 HOST_A2 HOST_A3 HOST_A4 HOST_A5 HOST_A6 HOST_A7 HOST_A8	AA0 AA1 AA2 AA3 AA4 AA5 AA6 AA7		BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7 BA8	SPHSF_A0 SPHSF_A1 SPHSF_A2 SPHSF_A3 SPHSF_A4 SPHSF_A5 SPHSF_A6 SPHSF_A7 SPHSF_A8
HOST_A9	AA9	6	BA9	SPHSF_A9
HOST_A10	AA 10	b	BA10	SPHSF_A10
HOST_A11	AA 11	4	BA11	SPHSF_A11
HOST_A12	AA 12	K	BA12	SPHSF_A12
HOST_A13	AA 13		BA13	SPHSF_A13
HOST_A14	AA 14	1	BA1 <del>4</del>	SPHSF_A14
HOST_A15	AA 15		BA15	SPHSF_A15
11001=7110	720	X	<i>D</i> , (10	017101 27110
HOST_RAM_READ_1	ARD	1	BRD	SPHSF_RAM_READ_01
HOST_RAM_WRITE_1	AWR		BWR	SPHAF_RAM_WRITE_01
LHD_0	AD0	6	BD0	SPHSF_DATA_32
LHD_1	AD1		BD1	SPHSF_DATA_33
LHD_2	AD2		BD2	SPHSF_DATA_34
LHD_3	AD3		BD3	SPHSF_DATA_35
LHD_4	AD4		BD4	SPHSF_DATA_36
LHD_5	AD5		BD5	SPHSF_DATA_37
LHD_6	AD6		BD6	SPHSF_DATA_38
LHD_7	AD7		BD7	SPHSF_DATA_39
LHD_8	AD8		BD8	SPHSF_DATA_40
LHD_9	AD9		BD9	SPHSF_DATA_41
LHD_10	AD10		BD10	SPHSF_DATA_42
LHD_11 LHD_12	AD11 AD12		BD11 BD12	SPHSF_DATA_43 SPHSF_DATA_44
LHD_13	AD13		BD13	SPHSF_DATA_45
LHD_14	AD14		BD14	SPHSF_DATA_46
LHD_15	AD15		BD15	SPHSF_DATA_47
	DUAL_	PORT	_RAM	

DUAL PORT RAM BITS 32 TO 47

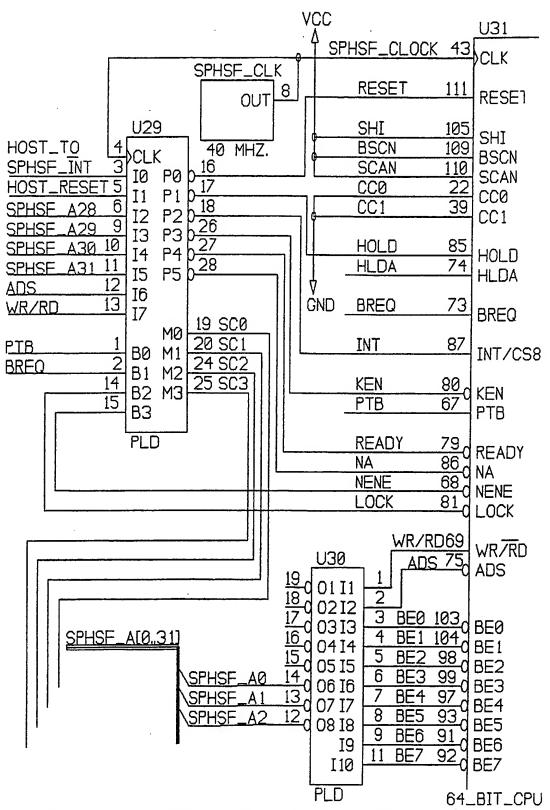
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FIG.12B

HOST_A[0.31]	HOST_DATA_[0,.31]				SPHSE_DATA_[0,.63]
HOST_A0	_HOST_A[0,31]	1100		•	SPHSF_A[0,31]
HOST_RAM_READ_1	H0ST_A1 H0ST_A2 H0ST_A3 H0ST_A4 H0ST_A5 H0ST_A6 H0ST_A7 H0ST_A8 H0ST_A9 H0ST_A9 H0ST_A10 H0ST_A11 H0ST_A12 H0ST_A13 H0ST_A14	AA1 AA2 AA3 AA5 AA6 AA7 AA8 AA10 AA11 AA12 AA13	4	BA1 BA2 BA3 BA4 BA5 BA6 BA7 BA8 BA9 BA10 BA11 BA12 BA13 BA14	SPHSF_A1 SPHSF_A2 SPHSF_A3 SPHSF_A4 SPHSF_A5 SPHSF_A6 SPHSF_A7 SPHSF_A8 SPHSF_A8 SPHSF_A9 SPHSF_A10 SPHSF_A11 SPHSF_A12 SPHSF_A13 SPHSF_A14
LHD_29   AD13   SPHSF_DATA_61   LHD_30   AD14   BD14   SPHSF_DATA_62   LHD_31   AD15   BD15   SPHSF_DATA_63   DUAL_PORT_RAM	HOST_RAM_WRITE_1  LHD_16  LHD_17  LHD_18  LHD_19  LHD_20  LHD_21  LHD_21  LHD_21  LHD_22  LHD_23  LHD_24  LHD_25  LHD_26  LHD_27  LHD_28  LHD_29  LHD_30  LHD_31	AWR AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD10 AD11 AD12 AD13 AD14 AD15	16.	BRD BWR BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7 BD8 BD10 BD11 BD12 BD13 BD14 BD15	SPHSF_RAM_READ_01 SPHAF_RAM_WRITE_01  SPHSF_DATA_48 SPHSF_DATA_49 SPHSF_DATA_50 SPHSF_DATA_51 SPHSF_DATA_52 SPHSF_DATA_53 SPHSF_DATA_53 SPHSF_DATA_55 SPHSF_DATA_55 SPHSF_DATA_56 SPHSF_DATA_57 SPHSF_DATA_58 SPHSF_DATA_59 SPHSF_DATA_60 SPHSF_DATA_61 SPHSF_DATA_62

DUAL PORT RAM BITS 48 TO 63

*وراہو* FIG.13A



SPECIAL PURPOSE HIGH SPEED FUNCTION

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: FIG.13B

	U31		SPHSF_DATA_[063]
	·	D0 D1 D2 D3 D4 D5 D6 D7	116 SPHSF_DATA_0 115 SPHSF_DATA_1 132 SPHSF_DATA_2 131 SPHSF_DATA_3 147 SPHSF_DATA_4 130 SPHSF_DATA_5 163 SPHSF_DATA_6 129 SPHSF_DATA_7
		D8 D9 D10 D11 D12 D13 D14 D15	145 SPHSF_DATA_8 146 SPHSF_DATA_9 162 SPHSF_DATA_10 128 SPHSF_DATA_11 161 SPHSF_DATA_12 127 SPHSF_DATA_13 143 SPHSF_DATA_14 144 SPHSF_DATA_15
		D16 D17 D18 D19 D20 D21 D22 D23	160 SPHSF_DATA_16 126 SPHSF_DATA_17 159 SPHSF_DATA_18 142 SPHSF_DATA_19 158 SPHSF_DATA_20 125 SPHSF_DATA_21 141 SPHSF_DATA_22 124 SPHSF_DATA_23
64_BIT.	_CPU	D24 D25 D26 D27 D28 D29 D30 D31	157 SPHSF_DATA_24 140 SPHSF_DATA_25 156 SPHSF_DATA_26 123 SPHSF_DATA_27 139 SPHSF_DATA_28 122 SPHSF_DATA_29 138 SPHSF_DATA_30 121 SPHSF_DATA_31
	SPECIAL	PURPOSI	E HIGH SPEED FUNCTION

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FIG.13C

	. •	SPHSF_DATA_[0,63]
U31		
	D32 D33 D34 D35 D36 D37 D38 D39	120 SPHSF_DATA_32 114 SPHSF_DATA_33 107 SPHSF_DATA_34 108 SPHSF_DATA_35 101 SPHSF_DATA_36 102 SPHSF_DATA_37 100 SPHSF_DATA_38 96 SPHSF_DATA_39
	D40 D41 D42 D43 D44 D45 D46 D47	94 SPHSF_DATA_40 95 SPHSF_DATA_41 89 SPHSF_DATA_42 90 SPHSF_DATA_43 88 SPHSF_DATA_44 83 SPHSF_DATA_45 82 SPHSF_DATA_46 84 SPHSF_DATA_47
	D48 D49 D50 D51 D52 D53 D54 D55	76 SPHSF_DATA_48 77 SPHSF_DATA_49 70 SPHSF_DATA_50 78 SPHSF_DATA_51 64 SPHSF_DATA_52 71 SPHSF_DATA_53 65 SPHSF_DATA_54 72 SPHSF_DATA_55
64_BIT_CPU	D56 D57 D58 D59 D60 D61 D62 D63	58 SPHSF_DATA_56 66 SPHSF_DATA_57 59 SPHSF_DATA_58 53 SPHSF_DATA_59 37 SPHSF_DATA_60 60 SPHSF_DATA_61 38 SPHSF_DATA_62 54 SPHSF_DATA_63

SPECIAL PURPOSE HIGH SPEED FUNCTION

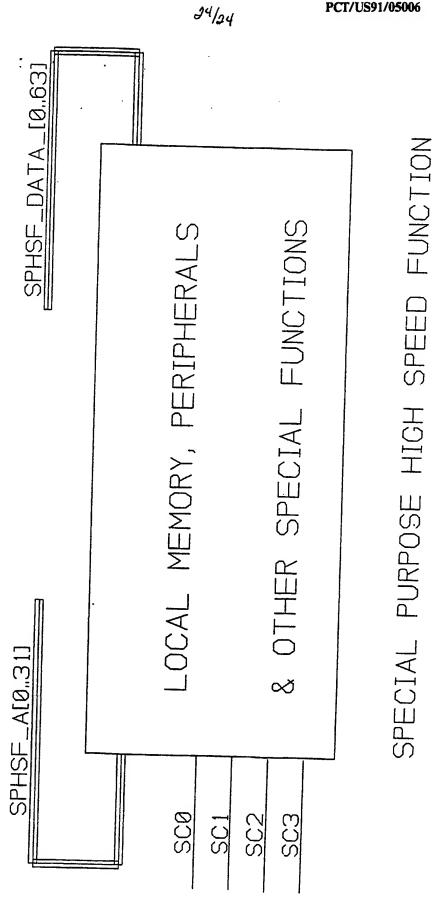
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: FIG.13D

SPHSF_A[031]	
	U31
SPHSF_A3 61	42
SPHSF_A4 62	4 A3
SPHSF_A5 55	1 A4
SPHSF_A6 49	A5
SPHSF_A7 48	1.A6
SPHSF_A8 31	4 A7
SPHSF_A9 47	A8
SPHSF_A10 30	A9
SPHSF_A11 46	A 10
SPHSF_A12 13	A11
SPHSF_A13 29	A12
SPHSF_A14 45	A13
SPHSF_A15 28	A14
SPHSF_A16 44	A 15
SPHSF_A17 12	A 16
SPHSF_A18 27	A 17
SPHSF_A19 11	A 18
SPHSF_A20 26	A 19
SPHSF_A21 10	A20
SPHSF_A22 42	A21 A22
SPHSF_A23 9	A22 A23
SPHSF_A24 25	A24
SPHSF_A25 8	A21 A25
SPHSF_A26 41	A26
SPHSF_A27 24	A27
SPHSF_A28 23	A28
SPHSF_A29 7	A29
SPHSF_A30 40	A30
SPHSF_A31 6	A31
Ψ	64_BIT_CPU
	01-011-000

SPECIAL PURPOSE HIGH SPEED FUNCTION

FIG, 13E



SUBSTITUTE SHEET

# INTERNATIONAL SEARCH REPORT

International Application No PCT/US91/05006

I. CLAS	SIFICATION OF SUBJECT MATTER (if several car	ISSISCATION SYMBOLS AND INCIDENCE OF THE	0032703000				
	1. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 3  According to International Patent Classification (IPC) or to both National Classification apply  IPC (5): GOGE 13/00 15/20						
IFC (	IPC (5): G06F 13/00, 15/20 U.S. Cl. 395/325						
II FIELDS SEARCHED							
	· · · · · · · · · · · · · · · · · · ·						
Classificat	ion System j	mentation Searched 4					
	or of the state of	Classification Symbols					
r.s.	C1. 395/325,800						
	to the Extent that such Documen	er than Minimum Documentation nts are Included in the Fields Searched #					
III DOCE	MENTS CONSIDERED TO BE RELEVANT !-	· · · · · · · · · · · · · · · · · · ·					
Category *		ppropriate, of the relevant passages 17	Relevant to Claim No. 15				
Y	US, A, 4,246,637 (BROWN) 20 JA	1-11					
	Note (Fig. 1, element 22; Col. 2, lines 17-20.						
	Col. 3, lines 36-38)						
Y	IIS A 4 860 244 (RDIFFERDE) 22						
-	US, A, 4,860,244 (BRUCKERT) 22 Note (Abstract; Col. 2 and 3;	2–6					
	Note (Abstract, Cor. 2 and 3; Fig. 6)						
Y,P	US, A, 4,953,930 (RAMSEY) 04 SI	EPTEMBER 1990 (04.09.90)	7-9,11				
	Note (Col. 3, lines 18-36; Col.	. 2. lines 60 and 61:	7-9,11				
]	Abstract)						
	TIC A / FOI 070 (777777						
A	US, A, 4,591,973 (FERRIS, III)	1-11					
A	A US, A, 4,309,754 (DINWIDDIE, JR.) 05 JANUARY 1982						
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* Special	categories of cited documents; 13	"T" later document published after the	international filing date				
CONSI	considered to be of particular relevance or priority date and not in conflict with the application but cited to understand the principle or theory underlying the						
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"L" document which may throw doubts on priority claim(t) or which is cited to establish the publication date of souther.							
Cannot be considered to involve an inventive step when the							
other means  other means  other means  document is combined with one or more other such docu- ments, such combination belong obvious to a person skilled							
"P" document published prior to the international filing date but later than the priority date claimed in the art. "A" document member of the same patent family							
V. CERTIFICATION							
Date of the Actual Completion of the International Search 3		Date of Mailing of this International Search Report 3					
		11 DEC 1991					
International Countries Authority							
nternational Searching Authority 1 Signature of Authorized Officer 29 Mg off o Nguyeu							
ISA/US INTERNATIONAL DIVISIO							
		AN GOLUM O. WHI	· · · · · · · · · · · · · · · · · · ·				